## AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

### Listing of Claims:

1. (Previously Presented) A predistortion digital linearizer, comprising:

a predistorter coupled to receive an input signal and a control signal to generate a predistorted signal;

an up-converter coupled to receive the predistorted signal and convert it into a radio frequency signal;

a high power amplifier (HPA) to receive and amplify the radio frequency signal outputted from the up-converter;

a feedback unit coupled to receive an output of the HPA and down-convert the received signal into a baseband signal;

an adaptation processing unit coupled to receive the baseband signal and a delayed digital input signal to generate the control signal, the adaptation processing unit including:

a delay unit to delay the input signal for a prescribed period of time; and a digital signal processor coupled to receive the delayed input signal and the baseband signal from the feedback unit to generate the control signal, wherein the predistorter comprises:

a power measuring unit to measure a power magnitude of the input signal;

a work function generator to receive an output of the power measuring unit and the control signal and to generate a predistortion work function for determining a distortion size of the input signal according to the magnitude of the input signal; and

a complex coupler to receive and complex-couple the predistortion work function and the input signal to generate the predistorted signal.

2. (Canceled)

3. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the power measuring unit comprises:

a first square unit to square a first phase digital input signal and output a first square value;

a second square unit to square a second phase digital input signal and output a second square value; and

an adder configured to add the first and second square values to obtain a magnitude of the input signal.

4. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the work function generator comprises:

a first square unit to square the power measured by the power measuring unit to generate a first square value;

a first coefficient multiplier to multiply the first square value with a first coefficient value outputted from the adaptation processing unit;

a second coefficient multiplier for multiplying the power measured by the power measuring unit with a second coefficient value outputted from the adaptation processing unit;

a first adder to add outputs of the first and the second coefficient multipliers and a third coefficient value outputted from the adaptation processing unit to form a first predistortion work function;

a second square unit to square the power measured by the power measuring unit to generate a second square value;

a third coefficient multiplier to multiply the second square value with a fourth coefficient value outputted from the adaptation processing unit;

a fourth coefficient multiplier to multiply the power measured by the power measuring unit with a fifth coefficient value outputted from the adaptation processing unit; and

a second adder to add the outputs of the third and the fourth coefficient multipliers and a sixth coefficient value outputted from the adaptation processing unit to form a second predistortion work function.

5. (Previously Presented) The predistortion digital linearizer of claim 4, wherein the first predistortion work function corresponds to a first phase of the input signal, and wherein the second predistortion work function corresponds to a second phase of the input signal.

6. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the complex coupler comprises:

a first multiplier to multiply a first phase digital input signal with a first work function;

a second multiplier to multiply a second phase digital input signal with the first work function;

a third multiplier to multiply the second phase digital input signal with the second work function;

a fourth multiplier to multiply the first phase digital input signal with the second work function;

a subtracter to subtract an output of the first multiplier from an output of the third multiplier to distort the first phase digital input signal; and

an adder to add an output of the second multiplier to an output of the fourth multiplier to distort the second phase digital input signal.

7. (Previously Presented) A predistortion digital linearizer, comprising:

a predistorter coupled to receive an input signal and a control signal to generate a predistorted signal;

an up-converter coupled to receive the predistorted signal and convert it into a radio frequency signal;

a high power amplifier (HPA) to receive and amplify the radio frequency signal outputted from the up-converter;

a feedback unit coupled to receive an output of the HPA and down-convert the received signal into a baseband signal;

an adaptation processing unit coupled to receive the baseband signal and a delayed digital input signal to generate the control signal;

a local oscillator to generate a local frequency for modulation and demodulation at the up-converter and the feedback unit;

a directional coupler configured to split the output of the HPA in a prescribed ratio; and

a terminator to terminate an end of a transmission line to prevent reflection of the output signal of the HPA that has passed the directional coupler.

8. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the input signal is a digital input signal and the predistorted signal is a predistorted digital signal, and wherein the up-converter comprises:

first and second digital-to-analog converters to convert the predistorted digital signal to an analog signal; and

a modulator to modulate the analog signal outputted from the digital-to-analog converters.

9. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the feedback unit comprises:

a demodulator to demodulate the output of the HPA; and

first and second analog-to-digital converters to convert the demodulated analog signal outputted from the demodulator to a digital signal.

10. (Canceled)

11. (Previously Presented) A predistortion digital linearizer comprising:

a gain control circuit to receive an input signal and control a gain of the input signal according to a gain control signal, and output a gain controlled input signal;

a predistorter to receive the gain controlled input signal and a control signal to generate a predistorted signal;

an up-converter coupled to receive the predistorted signal and convert it into a radio frequency signal;

a high power amplifier (HPA) to receive and amplify the radio frequency signal outputted from the up-converter;

a feedback unit coupled to receive an output of the HPA and down-convert the received signal into a baseband signal;

an adaptation processing unit coupled to receive the baseband signal and a delayed digital input signal to generate the control signal, the adaptation processing unit including:

a delay unit to delay the input signal for a prescribed period of time, and

a digital signal processor coupled to receive the delayed input signal and the baseband signal from the feedback unit to generate the control signal.

12. (Previously Presented) The predistortion digital linearizer of claim 11, wherein a gain of the gain control signal is set according to a gain of the delayed input signal, an output level of the HPA estimated by using the feedback digital output signal, and a desired HPA output level.

13. (Previously Presented) The predistortion digital linearizer of claim 11, wherein the gain control signal can be provided by the adaptation processing unit and can be provided by an external source.

14. (Previously Presented) The predistortion digital linearizer of claim 11, wherein the gain control circuit comprises:

a first multiplier to multiply a first phase digital input signal with the gain control signal to control a level of the first phase digital input signal;

a first rounding unit to remove a prescribed number of bits from a digital output signal of the first multiplier and adjust input and output digits;

a second multiplier to multiply a second phase digital input signal with the gain control signal and control a level of the second phase digital input signal; and

a second rounding unit to remove the prescribed number of bits from a digital output signal of the second multiplier and adjust input and output digits.

15. (Previously Presented) The predistortion digital linearizer of claim 14, wherein the first and second rounding units maintain a sign bit of corresponding outputs of the first and second multipliers, and removes a prescribed number of lower bits from the corresponding outputs.

16. (Previously Presented) The predistortion digital linearizer of claim 1, wherein the predistorted digital signal has a distortion characteristic that is opposite of a distortion characteristic of the HPA, such that an output of the HPA is substantially non-distorted.

17. (Previously Presented) The predistortion digital linearizer of claim 1, wherein each of the input signal, the predistorted signal, and the baseband signal is a digital signal.

18. (Previously Presented) A predistortion digital linearizer, comprising:

a digital predistorter to distort a digital input signal according to a control signal, the digital input signal comprising first and second digital input signals, the first digital input signal having a different phase than the second digital input signal, and wherein the digital predistorter separately distorts the first and second digital input signals to provide first and second output signals, the digital predistorter including:

a power measuring unit to measure a power magnitude of the input signal,

a work function generator configured to receive an output of the power measuring unit and the control signal and configured to generate a predistortion work function for determining a distortion size of the input signal according to the magnitude of the input signal, and

a complex coupler configured to receive and complex-couple the predistortion work function and the input signal to generate the first and second output signals;

a digital-to-analog converter comprising first and second digital-to-analog converters to convert the respective output signals of the digital predistorter to analog signals;

a modulator coupled to modulate an output signal of the digital-to-analog converter to a frequency of a carrier;

a high power amplifier (HPA) coupled to power-amplify an output signal of the modulator;

a demodulator coupled to receive an output signal of the HPA and demodulate it to a baseband signal;

an analog-to-digital converter coupled to convert the analog baseband signal outputted from the demodulator to a digital signal, the analog-to-digital converter comprising first and second analog-to-digital converters to convert first and second analog baseband signals to first and second digital feedback signals; and

a digital signal processor coupled to compare an output signal of the analog-to-digital converter to the digital input signal and generate the control signal to control a distortion degree of the digital predistorter, wherein the digital signal processor uses each of the first and second digital feedback signals to generate the control signal.

19. (Previously Presented) The predistortion digital linearizer of claim 18, wherein the predistorted digital signal has a distortion characteristic that is opposite of a distortion characteristic of the HPA, such that an output of the HPA is substantially non-distorted.

20. (Previously Presented) The predistortion digital linearizer of claim 18, further comprising a coupler to receive and split off a portion of the output signal of the HPA and provide the split off portion to the demodulator.

21. (Canceled).

22. (Previously Presented) The predistortion digital linearizer of claim 18, wherein the digital signal processor generates first and second control signals to control each of the first and second digital input signals separately.

23. (Original) A predistortion digital linearizer, comprising:

a gain control circuit to receive and control a level of a digital input signal according to a gain control signal;

a predistorter coupled to predistort the gain controlled digital input signal in accordance with a control signal;

a digital-analog converter coupled to convert the predistorted digital signal to an analog signal;

a modulator coupled to modulate the analog signal outputted from the digital-analog converter;

a high power amplifier (HPA) coupled to power-amplify an output of the modulator;

a demodulator coupled to demodulate the amplified signal outputted from the HPA;

an analog-digital converter coupled to convert an analog baseband signal outputted from the demodulator to a digital signal;

a delay circuit coupled to delay the digital input signal for a prescribed period of time; and

a digital signal processor coupled to receive the output signal of the analog-digital converter and an output of the delay circuit to generate the gain control signal and the control signal.

24. (Previously Presented) The predistortion digital linearizer of claim 23, wherein the gain control circuit comprises:

a first multiplier to multiply a first phase digital input signal with the gain control signal to control a level of the first phase digital input signal;

a first rounding unit to take a prescribed number of bits from a digital output signal of the first multiplier and adjust input and output digits;

a second multiplier to multiply a second phase digital input signal with the gain control signal and control a level of the second phase digital input signal; and

a second rounding unit to take the prescribed number of bits from a digital output signal of the second multiplier and adjust input and output digits.

25. (Previously Presented) The predistortion digital linearizer of claim 23, wherein the predistorter comprises:

a first squaring unit to output a square value of a first phase digital input signal;

a second squaring unit to output a square value of a second phase digital input signal;

a first adder to add outputs of the first and the second square units to obtain a power of the digital input signal;

a third squaring unit to output a square value of an output of the first adder;

a first coefficient multiplier to multiply an output of the third square unit with a first coefficient value from the digital signal processor;

a second coefficient multiplier to multiply the output of the first adder with a second coefficient value from the digital signal processor;

a second adder to add outputs of the first and the second coefficient multipliers and a third coefficient value from the digital signal processor to output a first predistortion work function;

a fourth squaring unit to output a square value of the output of the first adder;

a third coefficient multiplier to multiply an output of the fourth square unit with a fourth coefficient value from the digital signal processor;

a fourth coefficient multiplier to multiply the output of the first adder and a fifth coefficient value from the digital signal processor;

a third adder to add outputs of the third and the fourth coefficient multipliers and a sixth coefficient value from the digital signal processor to output a second predistortion work function;

a first multiplier to multiply the first phase digital input signal and the first predistortion work function;

a second multiplier to multiply the second phase digital input signal and the first predistortion work function;

a third multiplier to multiply the second phase digital input signal and the second predistortion work function;

a fourth multiplier to multiply the first phase digital input signal and the second predistortion work function;

a subtracter to subtract an output of the first multiplier from an output of the third multiplier to distort the first phase digital input signal; and

a fourth adder to add an output of the second multiplier and an output of the fourth multiplier to distort the second phase digital input signal.

26. (Previously Presented) The predistortion digital linearizer of claim 23, wherein the digital signal processor is configured to adaptively control a gain and predistortion of the digital input signal according to an output level of the HPA, a delayed digital input signal, and a desired output level.

27. (Canceled)

28. (Previously Presented) A predistortion linearizer, comprising:

a gain control circuit to receive first and second digital input signals and control a gain of the first and second digital input signals according to a gain control signal, and output first and second gain controlled digital input signals;

a digital predistorter coupled to receive the first and second gain controlled digital input signals and a digital control signal to generate first and second digital conditioned signals having a prescribed distortion characteristic;

an amplifier circuit coupled to receive the first and second digital conditioned signals, convert the digital signals to analog signals, modulate the analog signals, and amplify the modulated signal; and

a feedback circuit coupled to receive a portion of the amplified signal and delayed first and second digital input signals to generate the digital control signal, wherein the prescribed distortion characteristic is an inverse of a distortion characteristic of the amplifier circuit.

29. (Previously Presented) The predistortion linearizer of claim 28, wherein the digital predistorter comprises:

a power measuring unit to measure a power magnitude of the first and second digital input signals;

a work function generator configured to receive an output of the power measuring unit and the digital control signal, and configured to generate a predistortion work function to determine a distortion size of the digital input signals according to a magnitude of the digital input signals; and

a complex coupler configured to receive and complex-couple the predistortion work function and the digital input signals to generate the first and second digital conditioned signals.

30. (Previously Presented) The predistortion linearizer of claim 29, wherein the power measuring unit comprises:

a first square unit to square the first digital input signal and output a first square value;

a second square unit to square the second digital input signal and output a second square value; and

an adder configured to add the first and second square values to obtain a magnitude of the digital input signal.

31. (Previously Presented) The predistortion linearizer of claim 29, wherein the work function generator comprises:

a first square unit to square the power measured by the power measuring unit to generate a first square value;

a first coefficient multiplier to multiply the first square value with a first coefficient value outputted from the feedback circuit;

a second coefficient multiplier for multiplying the power measured by the power measuring unit with a second coefficient value outputted from the feedback circuit;

a first adder to add outputs of the first and the second coefficient multipliers and a third coefficient value outputted from the feedback circuit to form a first predistortion work function;

a second square unit to square the power measured by the power measuring unit to generate a second square value;

a third coefficient multiplier to multiply the second square value with a fourth coefficient value outputted from the feedback circuit;

a fourth coefficient multiplier to multiply the power measured by the power measuring unit with a fifth coefficient value outputted from the feedback circuit; and

a second adder to add the outputs of the third and the fourth coefficient multipliers and a sixth coefficient value outputted from the feedback circuit to form a second predistortion work function.

32. (Previously Presented) The predistortion linearizer of claim 31, wherein the first predistortion work function corresponds the first digital input signal, and wherein the second predistortion work function corresponds to the second digital input signal.

33. (Previously Presented) The predistortion linearizer of claim 29, wherein the complex coupler comprises:

a first multiplier to multiply the first digital input signal with a first work function;

a second multiplier to multiply the second digital input signal with the first work function;

a third multiplier to multiply the second phase digital input signal with the second work function;

a fourth multiplier to multiply the first phase digital input signal with the second work function;

a subtracter to subtract an output of the first multiplier from an output of the third multiplier to distort the first phase digital input signal; and

an adder to add an output of the second multiplier to an output of the fourth multiplier to distort the second phase digital input signal.

34. (Previously Presented) The predistortion linearizer of claim 28, further comprising:

a local oscillator to generate a local frequency for modulation and demodulation at the up-converter and the feedback unit;

a directional coupler configured to split the output of the amplifier circuit in a prescribed ratio; and

a terminator to terminate an end of a transmission line to prevent reflection of the output signal of the amplifier circuit that has passed the directional coupler.

35. (Previously Presented) The predistortion linearizer of claim 28, wherein the feedback circuit comprises:

a demodulator coupled to receive and demodulate an output of the amplifier circuit;

first and second analog-to-digital converters coupled to convert a demodulated signal outputted from the demodulator into a baseband digital signal; and

a digital signal processor coupled to receive the baseband digital signal and delayed fist and second digital input signals to generate the digital control signal.

36. (Canceled).

37. (Previously Presented) The predistortion linearizer of claim 28, wherein a gain of the gain control signal is set according to a gain of a delayed first and second digital input signals, an output level of the amplifier circuit estimated by using a feedback signal, and a desired amplifier output level.